Revolutionary High Performance Interconnect Which Maximizes Signal Density

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ABSTRACT

Telecommunications, networking, and computer designers have requirements for future board to board interconnects to perform at sub-nanosecond risetimes and with higher signal densities. At the same time, there is a need for a cost effective interconnect method that does not require special board considerations such as gold plated pads or restrictive flatness specifications. Teradyne Connection Systems has developed a right angle board to board connector with integrated shielding which allows 100% of the pins to be used for signals while minimizing crosstalk and reflections. The complete pin utilization allows for higher bandwidth to be passed through a given board space. Comparable bandwidth through traditional connectors can only be achieved by increasing the number of pins used and grounding more pins. This approach requires a larger connector thereby taking up more board space and can still compromise signal integrity.

The interconnect that was developed by Teradyne gives 100 real signals per linear inch down to sub-500ps risetimes for single-ended applications. Due to the unique integrated shielding incorporated by this connector, the crosstalk contribution for distant lines drops off dramatically, therefore this connector is ideally suited for simultaneously switching applications. The internal construction of this connector is such that the signals are more closely coupled to the ground shield than they are to each other. This gives a low crosstalk solution at fast risetimes without sacrificing signal density. Another feature of this connector is that the backplane portion of the connector also incorporates integrated shielding. This results in a connector where the signals are well shielded from each other all the way down to the board where shielding in traditional products stops at the daughtercard/backplane interface. Various PWB launch configurations were considered during the design process and have been both modeled and measured during the optimization of the design. This lead to a unique construction of the connector whereby different portions of the connector were optimized to different impedances . This resulted in a connector with very good impedance characteristics.

Teradyne Connection Systems has also developed a unique connector which is optimized for differential applications. Special measures were taken to reduce crosstalk and skew within the pair. In order to reduce the "in pair" skew care was taken to make the line length's of the pair as close as possible. The differential connector, much like the single ended connector, has an integrated shielding mechanism which helps in reducing crosstalk. It is also very well impedance matched. This connector can support up to 50 differential pairs per linear inch.

This paper will provide more detail about the interesting attributes of this revolutionary interconnect solution, and will also describe the modeling and measurement techniques used analyze it.

Background

In late 1995 and into early 1996 Teradyne Connection Systems performed a survey of the major Telecommunications, Networking and Computer OEM’s for their future board-to-board interconnect needs. The results of the survey showed that the industry was headed in a direction that called for more advanced interconnect solutions.

In general the market which we surveyed described a need for a board to board interconnect, that would provide a substantial increase in signal densities while accommodating faster edge rates and improved signal integrity. (fig 1)

Computer System Designs Road Map

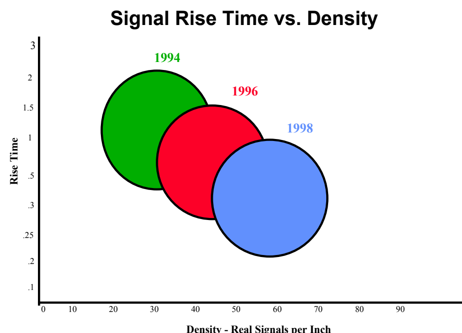

Figure 1

The traditional way of passing faster edge rates through a connector while maintaining acceptable signal integrity performance was to ground pins within the connector pin field. Ground pattern which had worked at 4:1 or 3:1 have been trending towards 2:1 or 1:1 to meet signal integrity needs. Industry is now looking for an interconnect solution to pass faster edge rates that has better signal integrity performance while providing a higher usable signal density. This demand is providing interconnect designers with new challenges that can overcome the effects of closely coupled signal pins and the added noise from faster edge rates. The need for higher signal speed and greater signal density is being driven primarily by the industries desire for increased bandwidth. The increased bandwidth requirements on the daughtercard side is being met by new high speed devices and advanced ASIC’s. The interconnect system has now become one of the “gates” in passing high speed system signals from daughtercards to backplanes. Teradyne Connection Systems Product Development will introduce a new connector design that meets the market needs of increased bandwidths.

Construction

To reach the speed and density requirements described previously, the internal construction of the interconnect to be altered from that of a traditional connector.

The faster digital pulses are comprised of higher frequency content waves, to achieve sharp rise and fall times. An approximation for the frequency content has been defined as .35/tr = frequency. For a 200ps signal this equates to a frequency of 1.75 GHz.

At this speed the connector and board interface becomes an appreciable percentage of the wavelength and must be treated as a transmission line. The system designers need for more real signals in addition to the impedance matching forced a paradigm shift in the construction and assembly of the connector. With this in mind, the internal construction of the interconnect would need to maintain a controlled impedance for as long as length as feasible. For differential signals, the lines within a pair ideally would be the same length.

Rather than modifying traditional open pin field connector to add external grounds or develop clever ways to fit shield plates into the pattern it was felt that for this effort the design would need to incorporate full internal shield plates between all columns of contacts and extending from board surface to board surface. The shield should also terminate in the boards in as close a proximity to the signal pins as is practical to avoid inductive ground return loops.

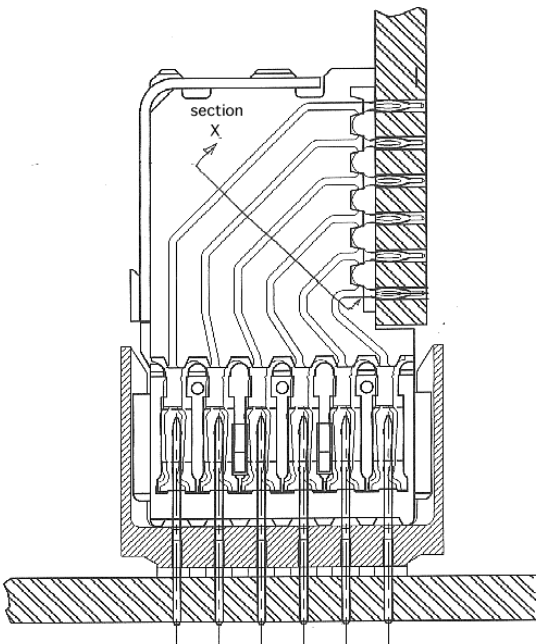

Figure 2

For impedance matching, section "X", (Figure 2) was matched to 50Ω while minimizing lead width and tuning distance to ground. This optimized geometry minimized crosstalk in this section allowing all contacts to be used as real signals. Additionally the connector impedance does not vary with selected ground pattern as would be true for a selectively grounded open pin field connector.

For differential signals the center section of the wafer was changed to increase the in pair coupling and at the same time increasing the pair to pair separation distance.

The inner lead of the pair was jogged to meet the outer lead in an effort to reduce the in pair skew (Figure 3).

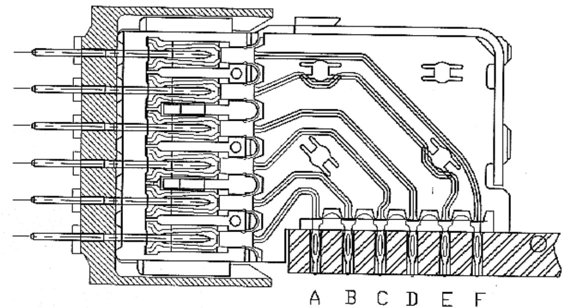

Figure 3

Termination's to the two P.C.B.'s were chosen to be compliant pin press fits. Electrically there was reason to consider SMT where the smaller vias would have reduced through hole capacitance. How ever for repairability boards flatness requirements, and solder inspection the press fit termination was chosen. To minimize the capacitance a new compliant (Figure 4) section has been developed for a smaller, .022" hole size.

Capacitance of via.
High Speed Digital Design,
Johnson/Graham Prentice Hall

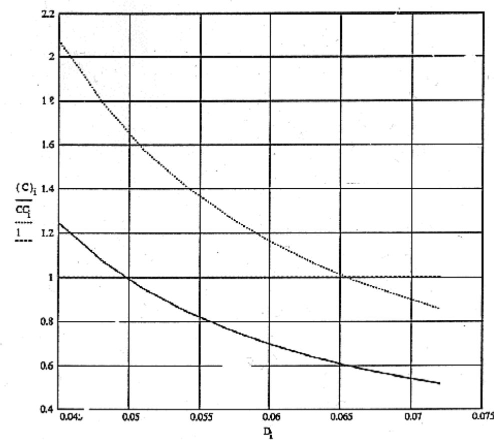

Figure 4

This reduced diameter hole also allows routing larger traces through the pattern (Figure 5). For example, with 1 oz copper signal layers, 2 track, .005" lines and spaces are possible.

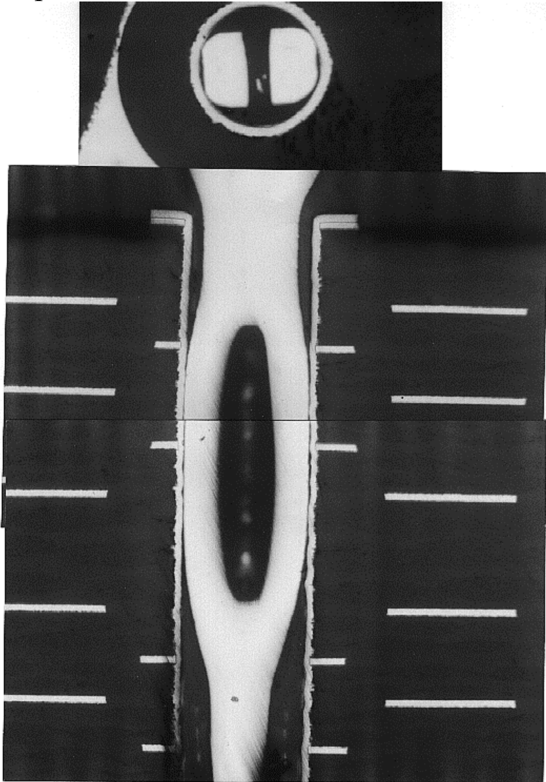

Figure 5

With an open pin field connector care must be taken when selecting a ground pattern as the multiple clearance holes for signal vias can leave only thin webs of ground trace between vias. This can lead to an appreciable increase in the crosstalk contribution of the footprint. The signals, as they pass out of the footprint have a substantial ground return to avoid "ground starvation".

Higher density connectors by definition have more contacts and inherently have correspondingly higher insertion forces. To minimize the impact this would have on a rack design, the connector was designed with a low springrate, preloaded contacts and a low entrance angle of the male pin.

The beam deflection was designed to accommodate normal assembly and component tolerances, defined here as the operating range. The lower springrate (K1) limits the variation of overall connector insertion force (Figure 6)

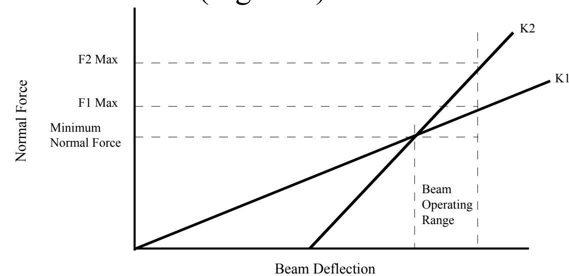

Figure 6

Modeling and Verification

As was seen in the previous section, this is a very complex connector. Modeling the connector presented a number of challenges. Some of the challenges included which method should be used to model the connector (FEM, MoM, BEM, etc.), 2D or 3D, which sections to model, etc. These issues are important in all modeling problems but in this case the decisions had to be made more carefully than in the past because of the signal speeds that were going to be passed through this connector. With the fast edge rates, which contain large portion of high frequency components, the ability to see the effects the high frequencies will have on the connector was very important.

One of the largest challenges in modeling this connector was to simulate any ringing that may occur due to the ground plates. The ringing could occur if the interface from the daughtercard shield to the backplane shield is not ideal. As can be

seen from Figure 8

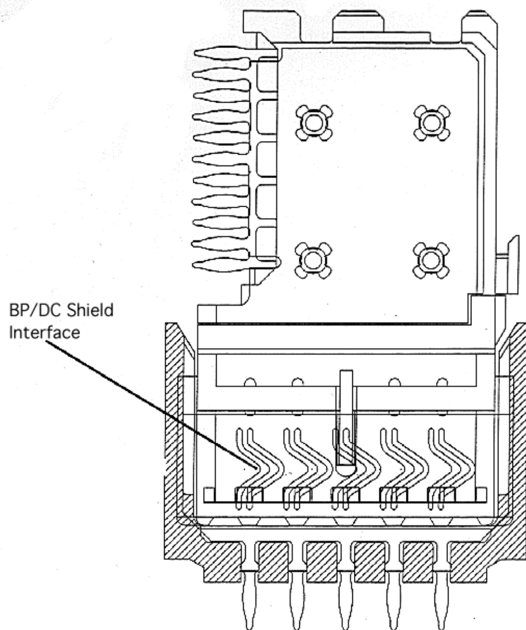

Figure 8

the ideal daughtercard shield mates with the ideal backplane shield at only five points for the six row connector. This convergence will cause the ground system to ring at high frequencies. Also, the shields have stubs which will contribute to the ringing. The ringing effect can be simulated by using 3D geometries or by carefully using 2D sections that will take into account all the stubs.
In the initial design of the connector many assumptions were made in trying to generate an electrical model of the connector. Ansoft's Maxwell software was used in generating the models and creating the SPICE deck. Applied Simulations ApSimSpice was used for the SPICE analysis. In the initial analysis of the connector the ground plane was assumed to be ideal and uniform. This was done in order to obtain the characteristic impedance of approximately 50 Ohms. The interface between the Daughtercard shield and the Backplane shield was also assumed to be ideal, this was done to simplify the model.

It turns out that the major contributor to the noise generated by this connector is in the portion of the interface where the backplane pins contact with the daughtercard receptacle Figure 9.

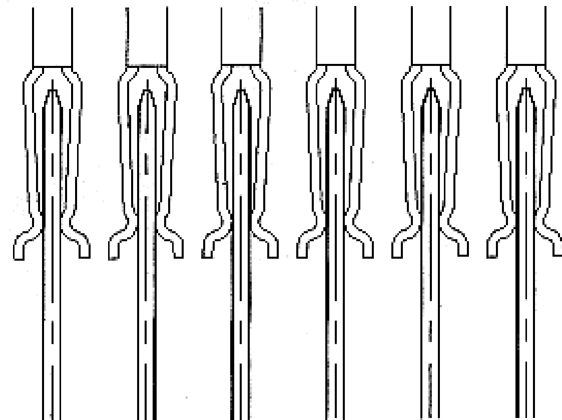

Figure 9

This "pin and socket" section is much larger in terms of width and they are much closer to each other thereby generating crosstalk on adjacent pins (Figure 10).

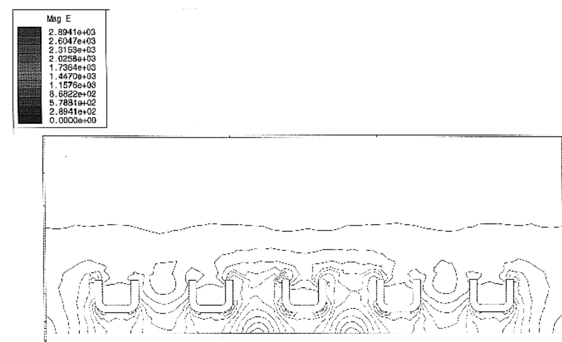

Figure 10

Also, because of their width the characteristic impedance is much lower in this section. The lower impedance creates a problem when trying to design the connector to 50 Ohms. The connector was designed to have a higher impedance (>50 Ohms) in the

right angle portion of the connector to offset the lower impedance at the pin and socket.

An increasingly important issue in high speed plated thru hole (PTH) connectors is the effect of the PTH itself on the overall impedance of the connector system. As the edge rates get faster the PTH becomes more "visible" in the reflection profile (Figure 11).

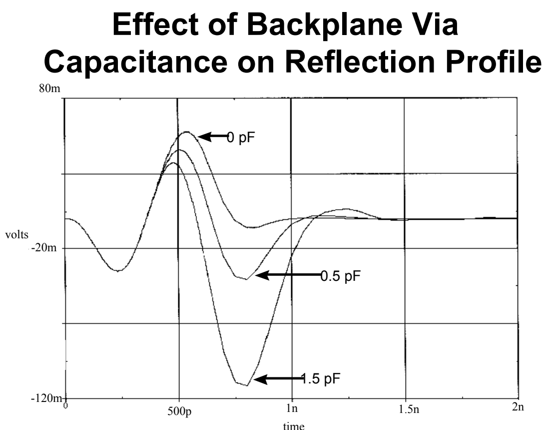

Figure 11

One way to combat this impedance issue with the PTH is to make the hole smaller in diameter thus reducing the surface area of the PTH. Surface mount connectors have a low PC terminated capacitance value which helps in reducing the impact on impedance. This is one of the over-riding issues in connector designs that incorporate PTH's especially when edge rates approach sub 300ps.

Measurements have confirmed that the shielded configuration when measuring multiline crosstalk are very low. For example, the connector measured at 300ps edge rates (10% - 90%) with ten nearest lines driven simultaneously give 7.5% backward crosstalk and -6.0% forward crosstalk. With this kind of performance the connector provides 100 "real" signals per inch. The Differential connector provides 50 signal pairs per inch and also has excellent signal integrity performance. At 200ps differential edge rates with 10 nearest pairs driven give 4.9% backward crosstalk and -3.8% forward crosstalk.

SUMMARY

A connector system was developed that eliminates the need to ground signal pins for signal integrity performance. This allows the use of all available pins for data transfer without sacrificing signal integrity performance.