

Signal Integrity Considerations for High Speed Data Transmission in a Printed Circuit Board System

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ABSTRACT:

As advances in microelectronics allow chips to increase in speed with additional I/O, printed wiring boards (PWB's) will be required to pass these higher density signals at faster edge rates. In typical system architectures, signals pass from a chip through a series of PWB's and connectors to a receiver. Although the signal transfer in personal computer motherboards is running busses at 66MHz, some servers and telecom equipment are passing data (point to point or differential) at speeds approaching 1 GHz. Because the risetimes are starting to approach the electrical length of the connections to internal layers, or plated through holes (PTH), the PTH's are starting to play a major role in the integrity of a signal. Plated through holes, or vias, have lower than desired impedances because of their inherent capacitance. Much of the system a signal travels in can be designed to meet desired impedances, however, PTH technology has not yet achieved this goal. The impedance mismatch from the PTH causes signal degradation due to reflections. In addition, PTH's in close proximity can be a source of crosstalk. Work has been done to develop a new type of signal "launch" into the PWB's that will maintain the mechanical benefits of large PTH's but also allow for signals greater than 1GHz to pass with minimal signal degradation. The focus of this paper will be on the effects of running these signals through the PWB system, and, in particular, comparing what happens to a signal as it passes through new PTH configurations.

I. INTRODUCTION:

Computer systems and other electronic equipment are commonly partitioned into subsystems on discrete Printed Wiring Boards (PWB's). These building blocks are typically multi layer boards with discrete layers dedicated to signal, power and ground. Consequently, PTH's are commonly used to connect signal traces from internal layers of a PWB to its surface for connection to devices or separable connector interfaces for connection to other boards. As faster signals are sent down through this trace-via-interface, the via geometry is now visible to the signal because it is of appreciable electrical length. Certain clearances and tolerances are required to cost effectively produce the PWB. This paper limits the majority of it's discussion to boards produced by common manufacturing processes and corresponding tolerances.

This paper explores the electrical effects of various geometric alterations to PTH's. With various PTH geometries consideration must be taken with respect to the amount of crosstalk generated from the PTH to traces running along side of it. The laminate material will not be varied from FR-4 for this discussion. This geometric comparison will be useful for a variety of laminate choices without considering the effects of altering the surrounding dielectric material. The capacitance should scale roughly proportional to the ratio of dielectric constraints.

$$[1] \quad C = \frac{1.41\epsilon T D_1}{D_2 - D_1}$$

Where

D_2 = diameter of clearance hole in ground plane(s), in.

D_1 = diameter of pad surrounding via, in.

T = thickness of printed circuit board, in.

ϵ_r = relative electric permittivity of circuit board material

C = parasitic via capacitance, pF

As board thickness or the diameter of the pad surrounding the via approaches zero, the through hole capacitance will also approach zero. In an attempt to be realistic in a range of capacitance reduction solutions simulations and measurement are for realistic interconnect methods. For compliant tail press fit, or solder PTH there is clearly a lower hole diameter limit currently around 0.020" diameter. Beyond this, the board itself becomes difficult to produce.

Smaller drills wander and break more easily and plating of the board holes becomes a challenge due to aspect ratio.

II. PWB Effects on Signal Integrity:

As data rates push beyond 2.5Gbits/sec the signal path from driver to receiver begins to play a major part in signal integrity performance. At these data rates every discontinuity in the data path contributes to the amount of crosstalk and reflection the signal will experience. A good example of this can be seen in Figure 1 where a TDR profile of the data path from one daughtercard through a backplane and back through another daughtercard is shown. (Figure 2).

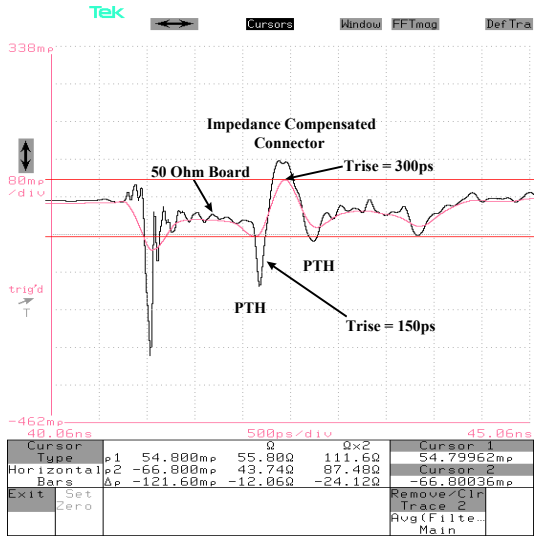


Figure 1: TDR Profile of Board, Connector and PTH's

In this example the major discontinuities are the daughtercard/backplane connectors, the plated through holes and the SMA connectors where the signals are launched from. As can be seen in Figure 1, the largest discontinuity comes from the plated through holes. The reason for this is that the PTH electrically looks like a lumped capacitor which lowers the impedance of the trace. Because of the lower impedance of the PTH, high speed connector designers try to compensate for the lower PTH impedance by increasing the connector impedance. Unfortunately, data rates are so fast that the connector can no longer compensate for the low PTH impedance. What this means to the connector and system designer is that the PTH must be taken into account and in some cases the PTH may need to be customized to meet the system impedance requirements.

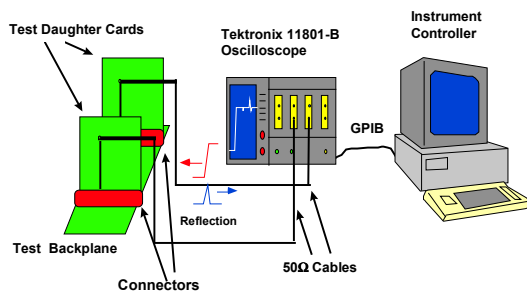


Figure 2: Test Set-up

There are several ways to make the connector/board interface less of a discontinuity at very fast

edge rates. The fundamental parameter that must be changed is the capacitance of the launch. An approach used as an alternative to a PTH is surface mount launches. However, surface mount launches do not guarantee that the launch capacitance will be any lower than a PTH. In fact the capacitance may be higher depending on the structure of the surface pad. For example the capacitance for an 0.028" finished hole in a 0.125" board is $\approx 1.1\text{pF}$ where for a surface mount launch like the one used for Teradyne's BOP connector the capacitance is measured to be $\approx 1.4\text{pF}$ in a similar board thickness. Another way to improve the signal integrity characteristics of the connector-board launch is to make the PTH as small as mechanically feasible. Using a smaller PTH in conjunction with expanding the ground clearance around the PTH will decrease the capacitance and thereby increase the characteristic impedance of the PTH (Figures 3a).

Board Thickness	Via Diam.	Gnd Clear.	Cap(pF)
0.1"	0.022"	0.042"	0.952
0.1"	0.022"	0.052"	0.722
0.1"	0.022"	0.062"	0.612

Figure 3a: Capacitance as a Function of Ground Clearance.

Board Thickness	Via Diam.	Gnd Clear.	Cap(pF)
0.150"	0.022"	0.052"	1.060
0.100"	0.022"	0.052"	0.722
0.050"	0.022"	0.052"	0.374

Figure 3b: Capacitance as a Function of Board Thickness.

Also, by using non-symmetric clearances, the PTH capacitance may be decreased (Figures 4a & b). When determining what type of via-pad geometry is optimal for a design, consideration must be taken for the expected thickness of the board. This can vary from an 0.062" daughtercard to 0.4" backplane. As shown in Figure 3b, given a particular via pad geometry, capacitance will vary greatly depending on the board thickness.

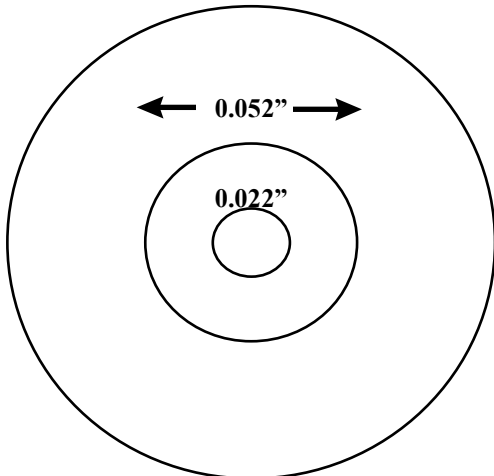


Figure 4a: 0.052 circular Gnd clearance with an 0.022" PTH gives a Cap. of 1.06pF

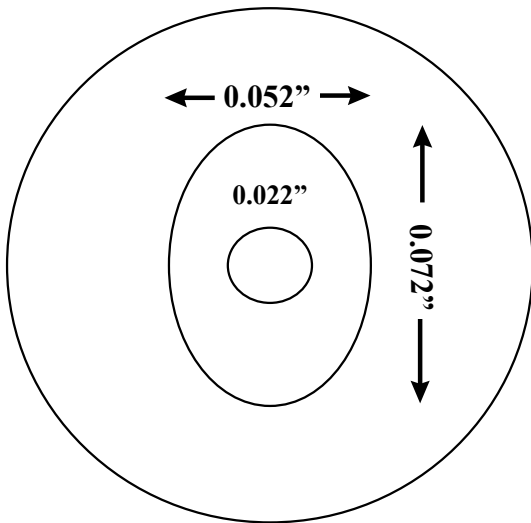


Figure 4b: Elliptical Gnd clearance with an 0.022" PTH gives a Cap. of 0.90pF

Another role that PTH's can play in effecting signal fidelity is crosstalk from a via to a signal passing by it. This can be a concern when the edge rates approach 100-150ps and/or the signal is going to track past a large number of PTH's. Figure 5 shows 3.3mV of crosstalk (generated out a 250mV signal at 150ps) as the signal passes through four footprints of an eight row connector.

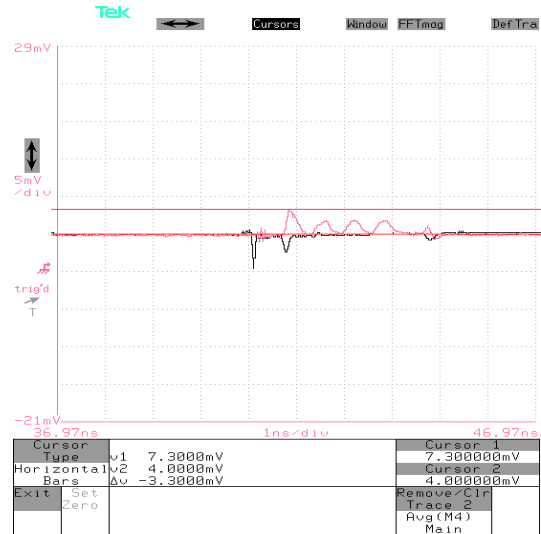


Figure 5: Crosstalk as signals pass by PTH's

Industry dictates faster signals in a smaller area despite the contradictory nature of the requirements. To run signals faster, tight control must be maintained over the characteristic impedance of the system and coupling must be minimized. The characteristic impedance and the degree of coupling are dependent on the geometry which is incompatible with size restrictions. Slight changes in plated through hole geometries will sufficiently satisfy both requirements to maintain signal speeds.

By altering the geometry of a plated through hole, impedance mismatches can be reduced with minimal impact on coupling. Expanding the ground clearances around a via reduces the capacitance of the barrel thus increasing the inherently low impedance of the plated through hole (Figure 3a). Expanding clearances, however, leads to traces being run over a perforated ground plane. Since running traces over a perforated ground plane can increase interlayer coupling this may not always be an ideal solution. However, depending on the spacing between traces and ground planes, a decreased ground web may not pose as much of a problem as one might think.

In order to see these effects, several simulations were performed using a finite-difference time-domain analysis. In order to create these models in three dimensions 120 slices were created in the xy plane and 50 slices were created in the xz plane. Slice 33 in the xz plane represents the

driven layer and slice 15 in the xz plane represents the quiet layer. Figures 6, 7, and 8 show two different configurations for a printed circuit board where two traces are routed between two plated through holes. In Figure 6 the traces being routed through the vias remain over the ground plane their entire travel, while in Figure 7 the traces travel over the clearances in the ground planes as they pass the vias. In order to see the effects of cross-talk from the PTH for the two cases, the plated through holes are excited on a separate layer from the victim traces. Two active lines drive the plated through holes on slice 33 in the xz plane (figs 9 and 10) but cannot be seen in the xy plane on slice 60 (fig 6 and 7). The active lines are driven from the bottom and the current travels along the edges of the traces as expected (Figures 9 and 10). Very little current continues past the via and to the other side of the driven line (the majority of the signal travels down the via.)

As the current travels through the via, very little electric field is coupled to the victim trace layer. The electric field remains within the driven layer for both the trace that runs over the clearance (Figure 6 - timesteps 4-7) and the trace that remains over the ground mesh (Figure 7 - timesteps 4-7). What little coupling that does occur on the victim layer is on the order of -9 to -12 dB for both cases. Figures 11 and 12 depict the victim layer and the electric field coupling from the vias to the traces. Unfortunately, the same time step pictures were not taken for both cases so it appears that more coupling occurs for the case “trace within the ground mesh” (fig 12). For the most part, the coupling from the PTH’s is the same, however, once the traces couple from the vias, the two traces couple more closely. The electric field remains between the two traces in Figure 12 for a much longer period of time due to the closer spacing of the traces.

Running traces over ground clearances has little or no effect in trace coupling from layer to layer in a pin-field. The coupling from signals on another layer through the PTH is more detrimental than the coupling between two traces through a clearance. The contribution of coupling from two traces running closely together for a long distance will be significantly more than the contribution from a short pass near a PTH.

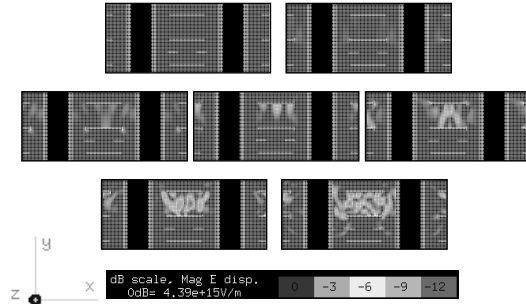


Figure 6: Magnitude of the Electric Field in the xy Plane. Center Slice, Trace over Clearance.

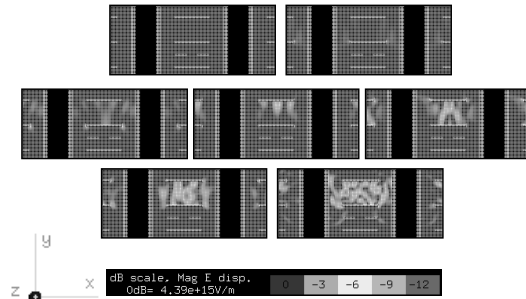
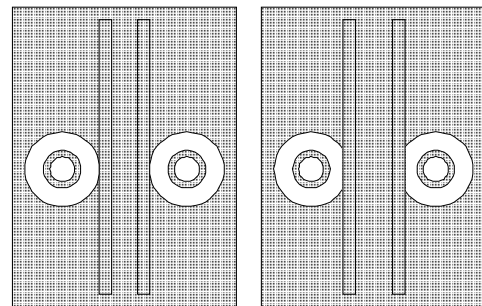


Figure 7: Magnitude of the Electric Field in the xy Plane. Center Slice, Trace within Ground Mesh.



Top down view: Traces next to clearances. Top down view: Traces over clearances.

Figure 8: Overhead view of trace layer and Ground Clearance.

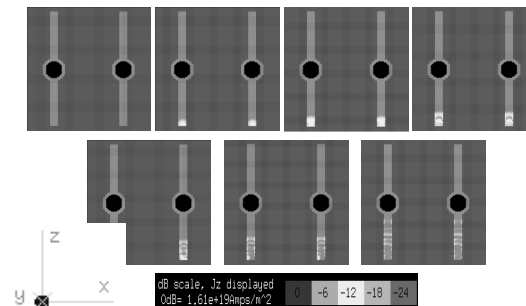


Figure 9: Current Density in the z Direction. Slice 33, Trace over clearance.

to be reviewed analytically to achieve an optimized low crosstalk, low reflection design.

III. References:

[1] Johnson, Howard and Martin Graham, "High-Speed Digital Design: A Handbook of Black Magic", Prentice Hall PTR, Upper Saddle River, New Jersey, 1993.

Kunz, Karl S. And Raymond J. Luebbers, "The Finite Difference Time Domain Method for Electromagnetics", CRC Press, Boca Raton, 1993.

Wadell, Brian C., "Transmission Line design Handbook", Artech House, Boston, 1991.

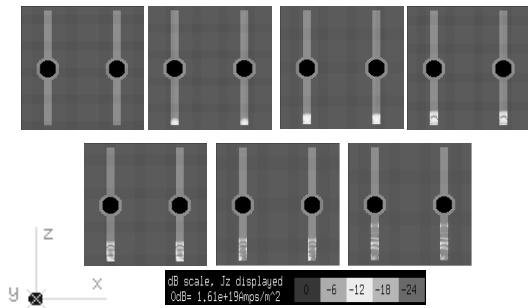


Figure 10: Current Density in the z Direction. Slice 33, Trace within ground mesh.

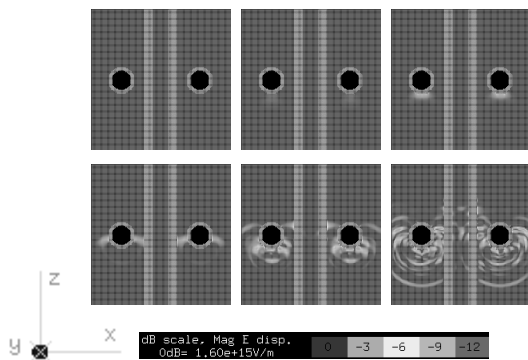


Figure 11: Magnitude of the Electric Field in the xz Plane. Slice 15, Trace over clearance.

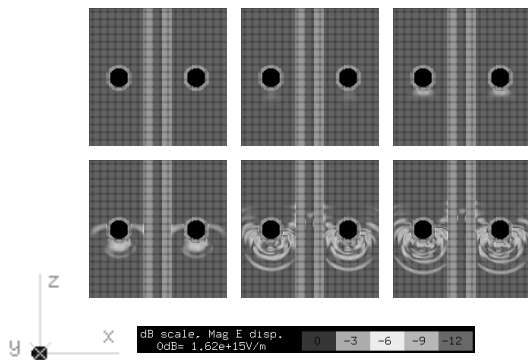


Figure 12: Magnitude of the Electric Field in the xz Plane. Trace within Ground Mesh.

III. Summary:

Many sections of a high speed signal path that were previously disregarded for analysis now have become significant and must be considered during system design. Fortunately there are some simple steps that can be taken to minimize detrimental effects. Additionally, at these speeds, old design rules or assumptions may need